Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**SOURCE**

**GATE**

**.125”**

**.179”**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: S = .023” X .036” G = .025” X .037”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .125” X .179” DATE: 7/7/17**

**MFG: SILICONIX THICKNESS .021” P/N: IRFC430**

**DG 10.1.2**

#### Rev B, 7/19/02